24th Year *1986-2010*

ADVANCE PROGRAM

2010 IEEE BIPOLAR / BiCMOS CIRCUITS AND TECHNOLOGY MEETING

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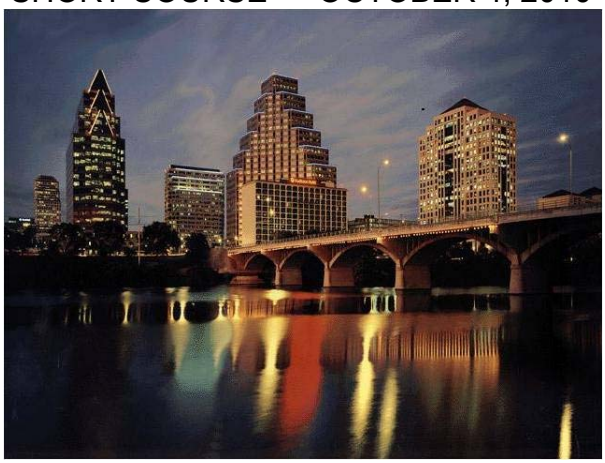
Radisson Hotel & Suites
Austin, Texas, USA

OCTOBER 5 – 6, 2010
SHORT COURSE — OCTOBER 4, 2010



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Bipolar/ BiCMOS Circuits and Technology Meeting BCTM 2010

Sub-com Invited Speakers

- RF Circuit Design:
  Professor Larry Larson (UCSD) – "4G Transceivers"

- Device Physics:
  Professor Leo de Vreede (TUDELFT) – "Design Concepts for Ultra-linear Varactor Circuits"

- Process Technology:
  Professor Choi (Yonsei University, Korea) – "Silicon Photo-Receivers"

- Modeling/Simulation:
  Larry Nagel – "SPICE History and Is SPICE Good Enough for Tomorrow's Analog?"

- Analog/Digital Circuit Design:
  Makoto Nakamura – "optical Rx for broadband access"

5. Integrated BiCMOS Components

Tuesday 2:00 PM **TRAVIS III**
Session Chair: **J. Donkers###**
Co-Chair: **G. Avenier**

(5.1) 2:00–2:50 PM **Silicon Integrated Photoreceivers (Invited)** **p. 77**

W.-Y. Choi, M.-J. Lee, J.-S. Youn

Integrated photoreceivers having photodetectors and necessary electronic circuits on the same chip are an essential element of high-performance optical interconnects. Various techniques for realizing integrated photoreceivers with the standard CMOS and BiCMOS technologies are reviewed.

(5.2) 2:50–3:15 PM **Hyperabrupt-Junction Varactor for mmWave SiGe:C BiCMOS, Enabling 77GHz VCO/TX with 13-15GHz Tuning Range** **p. 82**

V. P. Trivedi, J. Kirchgessner, J. P. John, P. Welch, D. Morgan, S. Stewart, R. Peterman, D. Hammock, J. Nivison, O. Hartin, S. Shams, I.-S. Lim, H. Li, S. Trotta, D. Salle, W. M. Huang

A millimeter-wave hyperabruptjunction varactor (HAVAR) enabling 77GHz VCO/TX with 13-15GHz tuning range and better than -70dBc/Hz phase noise at 100kHz offset has been integrated in SiGe:C BiCMOS for automotive radar products. The HAVAR predominantly uses existing processes for low-cost integration and minimal process complexity. Optimization of TR-Q through HAVAR width allows TR up to 2.7 and Q_{min} up to 10.

(5.3) 3:15–3:40 PM **Design and Optimization of Silicon JFET in 180nm RF/BiCMOS Technology** **p. 86**

Y. Shi, R. M. Rassel, R. A. Phelps, B. Rainey, J. Dunn, D. Harame

In this paper, we discuss a method to extrapolate intrinsic and extrinsic Ron component for a JFET. The results provide the guideline to lower Ron, hence to achieve competitive "R_{on} vs. pinch off (V_{off})" benchmark. The impacts on channel scaling and process variation are discussed. Besides, an improved RESURF condition is achieved using one of the experimental splits. The optimized JFET is demonstrated with 50% lower R_{on}, while maintaining low V_{off} , and BV_{dss} of 11 V.

(5.4) 3:40–4:05 PM **Integrated Si-LDMOS Transistors for 11 GHz X-Band Power Amplifier Applications** **p. 90**

R. Sorge, A. Fischer, A. Mai, P. Schley, J. Schmidt, Ch. Wipf, R. Pliquett and R. Barth

The integration of RF NLDMOS transistors into a 0.13 µm CMOS process for operating at X-Band (8.5-10.5 GHz) frequencies with over 11 dB gain and 0.25 W/mm power density and 22% power added efficiency at 1 dB output power compression is presented. The self aligned NLDMOS was modularly integrated into IHP's 130 nm SiGe BiCMOS platform targeting 1 W X-Band power amplifiers for radar and satellite communication applications.

Si Integrated Photoreceivers

Woo-Young Choi, Myung-Jae Lee, and Jin-Sung Youn

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***Abstract* — This paper reviews 850nm Si photodetectors and integrated photoreceivers realized with standard Si process technologies including CMOS and BiCMOS. Such photodetectors and photoreceivers are of great interest as they can provide cost-effective optical interconnect receiver solutions. High-speed integrated photoreceivers can be achieved by spatially modulated light, lateral PIN, and P^+/N-well junction photodetectors and their performances can be further enhanced with electronic equalizers, all of which can be realized with the standard Si technology.**

***Index Terms* — Avalanche photodetector, integrated optical receiver, optical interconnect, photodetector, photodiode, photoreceiver, Si avalanche photodetector, Si photodetector, Si photonics.**

I. Introduction

The data transmission requirements for many interconnect applications are continuously increasing. Existing electrical interconnects, however, face severe problems due to their link length limitation as well as increasing cross-talk noise and power consumption [1]. Recently, there are growing interests for optical interconnects based on Si photonics, which can overcome above problems [2]–[4].

In order to realize optical interconnects, implementation of high-performance and cost-effective photodetectors is required. In addition, there is a strong demand that such photodetectors should be integrated with electronic circuits on the same chip so that integrated photoreceivers can be realized. Ge-based photodetectors have been actively investigated because of their large absorption coefficient at 1.3-μm and 1.5-μm wavelengths as well as compatibility with present Si processing technologies [5], [6]. In fact, detection of 40-Gb/s optical data has been already achieved with Ge-based photodetectors [6]. It is expected integrated photoreceivers based on these Ge-based photodetectors will play an important role for high-speed optical interconnect applications.

However, there remains one interesting question: how good photoreceivers can we realize *without* any modification of the existing *standard* Si processing technologies? The structure of a photodetector is basically a PN junction, and the standard Si technology can provide several types of PN junctions that can detect 850-nm light. Of course, such photodetectors cannot escape limitations due to non-optimal device structures provided by the standard Si technology. But if their performances can be improved to a reasonable level with a careful selection of device structure as well as compensation with smart circuit techniques, they can immediately provide very cost-effective solutions for many applications. The fact that there exist cheap 850-nm optical transmission systems based on vertical-cavity surface-emitting lasers (VCSELs) and multimode fibers (MMFs) certainly helps in justifying this approach.

In this paper, various techniques are reviewed for realizing integrated photoreceivers with the standard Si processes including complementary metal-oxide-semiconductor (CMOS) and bipolar CMOS (BiCMOS) technologies. This paper is organized as follow. Section II describes structures of various photodetectors realized with standard CMOS technology and provides characteristics of CMOS integrated photoreceivers realized with those photodetectors. In Section III, high-performance monolithically integrated photoreceivers realized with standard SiGe BiCMOS technology is presented. In addition, performances of various Si integrated photo-receivers are compared.

II. Photodetectors and Integrated Photoreceivers in Standard CMOS Technology

The simplest way of realizing a photodetector with standard CMOS technology is using N-well/P-substrate junction as shown in Fig. 1 (a). It can provide wider depletion regions and, consequently, better detection efficiency than any other PN junctions available in standard CMOS technology. However, this type of photodetector is very slow with the photodetection bandwidth in the MHz range [7], and does not allow any high-speed applications. This is because many photons are absorbed in the region where photogenerated carriers experience slow diffusive transport.

The bandwidth performance can be significantly improved with electronic equalizers. As shown in Fig. 2, an equalizer is basically a high-pass filter that can compensate the low-pass filtering effect of a slow photodetector. By utilizing a finger-type N-well/P-substrate photodetector and an equalizer, [7] reported a photoreceiver that can achieve 3-Gb/s optical data

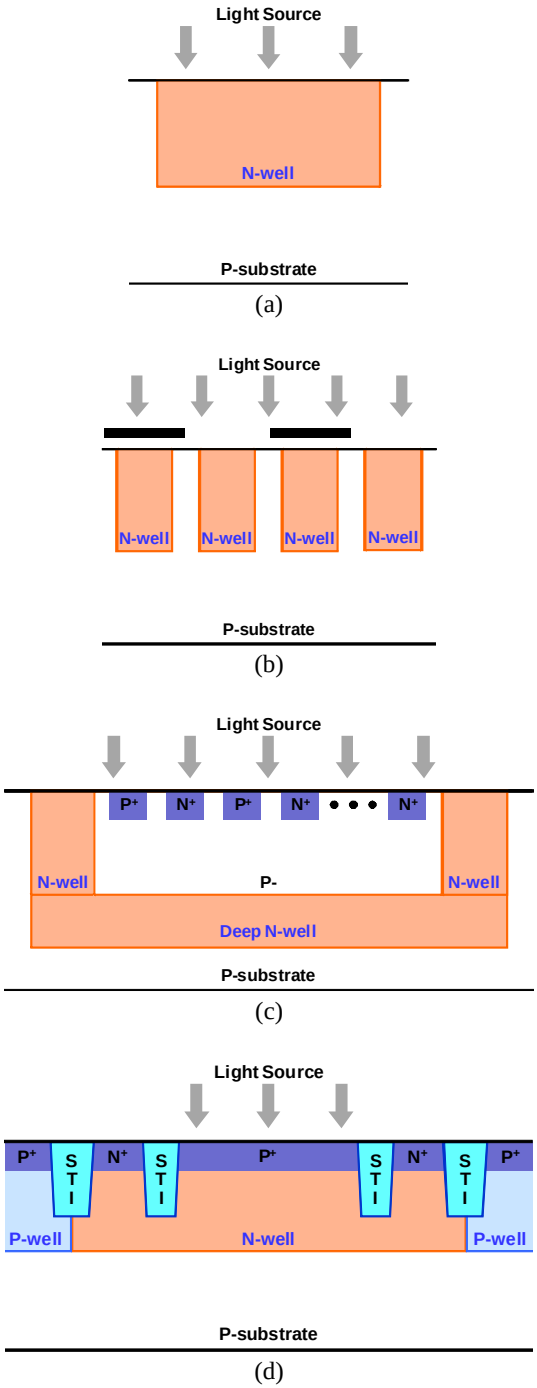

Fig. 1. Cross-sectional structures of Si photodetectors: (a) N-well/P-substrate, (b) spatially modulated light, (c) lateral PIN, and (d) P^+/N-well photodetectors.

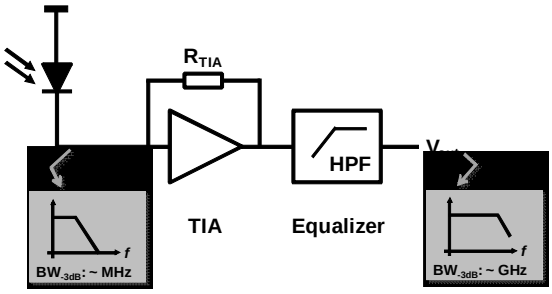

Fig. 2. Block diagram of integrated photoreceiver with an equalizer.

transmission. There have been continuous efforts to achieve larger intrinsic photodetection bandwidth, because equalizer circuits can be complex and the large photodetection bandwidth can be further enhanced by additional equalizer circuits. With spatially modulated light (SML) photodetectors, the photodetection bandwidth can be enhanced by excluding the slow diffusion components of the photodetectors [8], [9]. As shown in Fig. 1 (b), SML photodetectors are composed of a row of photodetectors alternatively covered and uncovered with light blocking materials, such as metal layers. Differential signaling is used to subtract slow diffusion components of covered regions from those of uncovered regions. SML photodetectors have larger photodetection bandwidth of about 500 MHz. With electronic equalizers, 3.125- and 4.5-Gb/s SML photoreceivers have been reported [8], [9].

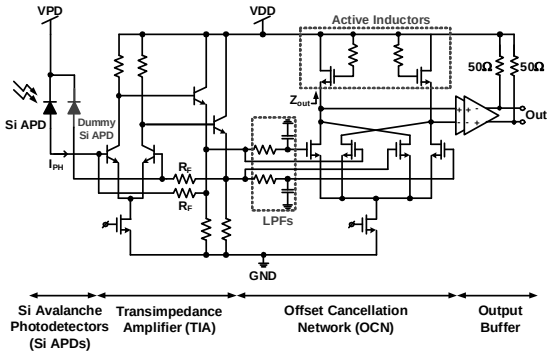

Fig. 4. Schematic of monolithically integrated BiCMOS photoreceiver front-end [13].

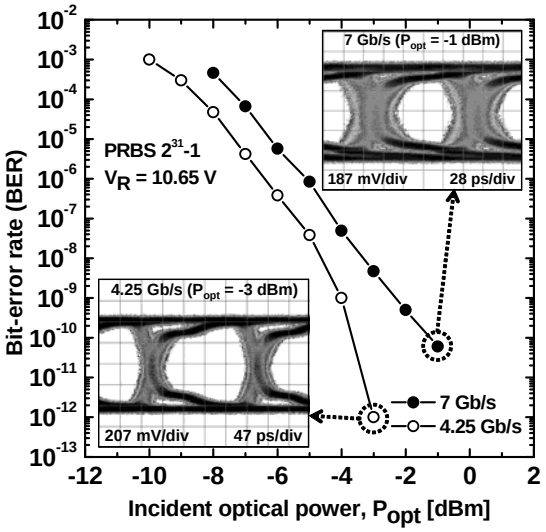

Fig. 5. BER versus incident optical power (P_{opt}). Inset shows the eye diagrams of 4.25-Gb/s and 7-Gb/s data at output of the limiting amplifier in BiCMOS photoreceiver [13].

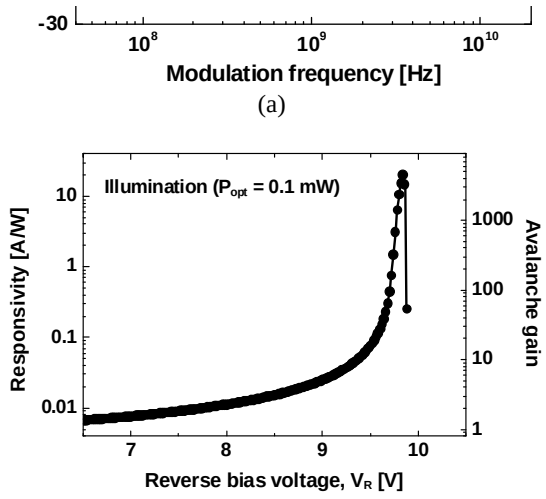

Fig. 3. (a) Photodetection frequency response of CMOS-APD. (b) Responsivity and avalanche gain of CMOS-APD as a function of the reverse bias voltage.

Another approach is using a lateral PIN structure, where P^+/P-substrate/N^+ regions are interleaved as shown in Fig. 1 (c) [10]. The photodetector is surrounded by N-well and Deep N-well regions, and photogenerated carriers created in the lateral depletion regions contribute to photocurrents. With this PIN photodetector, 2.5-Gb/s optical data was successfully detected without any equalizer circuits.

Another approach of enhancing photodetector bandwidth is using P^+/N-well junction, with which slow diffusion currents in P-substrate are eliminated. However, this structure suffers from reduced detection efficiency simply because the detection area is much reduced. We can solve this problem by using the avalanche gain. The structure of CMOS avalanche photodetector (CMOS-APD) is shown in Fig. 1 (d) [11]. The CMOS-APD has photodetection bandwidth of several GHz, and it has high detection efficiency due to the avalanche gain as shown in Fig. 3. Although the required bias voltage is larger than typical bias voltages, DC-DC converters can be used to generate the necessary bias voltages within the chip. We also found that STI plays an important role of providing strong electric fields in the planar junction periphery, alleviating any premature edge breakdown and, consequently, providing higher avalanche gain. An integrated photoreceiver having a CMOS-APD and TIA was realized with the standard CMOS technology and 4.25-Gb/s optical data was successfully transmitted without any equalizer [12].

III. Monolithically Integrated BiCMOS Photoreceiver Front-End

We have also investigated monolithically integrated photoreceivers fabricated with standard SiGe BiCMOS technology [13]. For the photodetector, we chose APD based on the same P^+/N-well structure as in CMOS technology, because additional PN junctions provided by the bipolar process do not improve photodetection characteristics since they have similar doping profiles as CMOS PN junctions. We have experimentally demonstrated, for example, that there is no appreciable performance difference between P^+/N-well junction and Base/Deep Collector junction APDs. However, the speed of the integrated photoreceiver can be enhanced since SiGe heterojunction bipolar transistors (HBTs) have large gain-bandwidth product than CMOS transistors.

Fig. 4 shows the simplified block diagram of our BiCMOS photoreceiver with an on-chip APD. The APD is realized with P^+/N-well junction. The TIA is

TABLE I
Performances of monolithically integrated photoreceivers fabricated with standard CMOS and BiCMOS technology

	[7]	[8]	[9]	[10]	[12]		[13]	
Technology	CMOS 0.18 μm	CMOS 0.18 μm	CMOS 0.13 μm	CMOS 0.18 μm	CMOS 0.13 μm		BiCMOS 0.25 μm	
Data rate	3 Gb/s	3.125 Gb/s	4.5 Gb/s	2.5 Gb/s	4.25 Gb/s	3.125 Gb/s	7 Gb/s	4.25 Gb/s
Sensitivity	-19 dBm	-4.2 dBm	-3.4 dBm	-4.5 dBm	-5.5 dBm	-8 dBm	-1 dBm	-3 dBm
BER (PRBS)	10^{-11} (2^{31}-1)	10^{-12} (2^{31}-1)	10^{-12} (2^{7}-1)	10^{-12} (2^{31}-1)	10^{-12} (2^{31}-1)		10^{-10} (2^{31}-1)	10^{-12} (2^{31}-1)
Receiver structure	N-well/P-sub +TIA+EQ	SML+TIA +EQ+LA	SML+TIA +EQ+LA	Lateral PIN +TIA+LA	P^+/N-well APD+TIA		P^+/N-well APD+TIA	

composed of two-stage differential amplifiers, implemented with HBTs. The offset cancellation network (OCN) having two low-pass filters (LPFs) and a f_T-doubler amplifier is used in order to convert pseudo- differential signals to fully differential. In addition, active inductors are included in OCN for the purpose of enhancing photoreceiver bandwidth.

Using the BiCMOS photoreceiver, optical data transmission experiments were performed. Optical signals from an 850-nm laser diode were modulated with a 2^{31}-1 pseudorandom bit sequence (PRBS) test pattern. The modulated optical signals were transmitted through 4-m-long MMF and injected into the photoreceiver using a lensed fiber. Fig. 5 shows measured bit-error rates (BERs) of received data as functions of input optical power (P_{opt}). 7-Gb/s optical data were successfully transmitted with BER of 10^{-10} at P_{opt} of -1 dBm. The insets of the Fig. 5 show the eye diagrams of 4.25-Gb/s and 7-Gb/s data at the output of the limiting amplifier.

Table I compares performances of CMOS and BiCMOS integrated photoreceivers reported in recent publications. In standard CMOS technology, various types of photodetectors based on N-well/P-substrate junction, SML, lateral PIN, and P^+/N-well junction photodetectors have been reported, and these photodetectors were monolithically integrated with CMOS electronic circuits [7]–[12]. The sensitivity of the N-well/P-substrate photoreceiver is better than others simply because the N-well/P-substrate junction absorbs more light. However, our CMOS-APD integrated photoreceiver shows better photodetection bandwidth without any equalizer circuits. In addition, the speed of the integrated photoreceiver can be further increased with SiGe BiCMOS technology as it provides better-performing transistors. The bandwidth of P^+/N-well photoreceivers can be further improved with electronic equalizers.

IV. Conclusion

Several techniques for realizing high-performance integrated photoreceivers with standard Si technologies are reviewed. Structures and performances of photodetectors based on SML, lateral PIN, and P^+/N-well junctions are briefly summarized. In addition, performances of integrated photoreceivers based on these photoreceivers are compared. We believe that, with further optimization of photodetector structures and circuit design techniques, the performance of Si photoreceivers realized with standard Si technologies can be further improved.

Acknowledgement

This work was supported in part by the IT R&D program of MKE/KEIT [002145] and Mid-career Researcher Program through NRF grant funded by the MEST [2010-0014798]. The authors are very thankful to IDEC for EDA software support. The integrated BiCMOS photoreceiver used in our investigation was fabricated with IHP 0.25-μm SiGe BiCMOS technology. The authors would like to thank Dr. H. Rücker in IHP for providing SiGe BiCMOS technology for this research.

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